**JK**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity jk\_Vedant is

port (

JK: IN STD\_LOGIC\_VECTOR(1 downto 0);

clock: IN STD\_LOGIC;

reset: IN STD\_LOGIC;

q: out STD\_LOGIC

);

end jk\_Vedant;

architecture jk\_Vedant\_arch of jk\_Vedant is

signal q\_s : std\_logic := '0';

begin

process(reset,clock)

begin

if (reset = '1')then

q\_s <='0';

elsif (clock'event and clock = '1')then

case (JK) is

when "00" => q\_s <= q\_s;

when "01" => q\_s <= '0';

when "10" => q\_s <= '1';

when others => q\_s <= not q\_s;

end case;

end if;

q <= q\_s;

end process;

end jk\_Vedant\_arch;

**JK TB**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.std\_logic\_unsigned.all;

USE ieee.numeric\_std.ALL;

ENTITY jk\_Vedant\_tb IS

END jk\_Vedant\_tb;

ARCHITECTURE behavior OF jk\_Vedant\_tb IS

COMPONENT jk\_Vedant

PORT(

clock : in std\_logic;

reset : in std\_logic;

count : out std\_logic\_vector(3 downto 0)

);

END COMPONENT;

SIGNAL clock : std\_logic := '0';

SIGNAL reset : std\_logic := '0';

SIGNAL count : std\_logic\_vector(3 downto 0);

BEGIN

uut: jk\_Vedant PORT MAP(

clock => clock,

reset => reset,

count => count

);

PROCESS

BEGIN

wait for 5ns;

clock <= not clock;

END PROCESS;

PROCESS

BEGIN

reset <= '1';

wait for 70ns;

reset <= not reset;

wait;

END PROCESS;

END;

**Asynchronous counter**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

use ieee.std\_logic\_arith.all;

entity async\_Vedant is

port(

rst,clk:In std\_logic;

o:Out std\_logic\_vector(2 downto 0)

);

end async\_Vedant;

architecture async\_Vedant\_arch of async\_Vedant is

component jk\_Vedant is

port(

JK:In std\_logic\_vector(1 downto 0);

reset:In std\_logic;

clock:In std\_logic;

q:Out std\_logic

);

end component;

signal s:std\_logic\_vector(2 downto 0);

begin

asc0:jk\_Vedant port map("11",rst,clk,s(0));

asc1:jk\_Vedant port map("11",rst,s(0),s(1));

asc2:jk\_Vedant port map("11",rst,s(1),s(2));

o<=s;

end async\_Vedant\_arch;

**ASYNC TB**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

use ieee.std\_logic\_arith.all;

entity async\_tb is

end async\_tb;

architecture async\_Vedant\_arch of async\_tb is

component async\_Vedant is

port(

rst,clk:In std\_logic;

o:Out std\_logic\_vector(2 downto 0)

);

end component;

signal rst,clk:std\_logic;

signal o:std\_logic\_vector(2 downto 0);

begin

uut:async\_Vedant port map(rst,clk,o);

process

begin

clk<='1';

wait for 10ns;

clk<=not clk;

wait for 10ns;

end process;

process

begin

rst<='1';

wait for 20ns;

rst<='0';

wait for 200ns;

end process;

end async\_Vedant\_arch ;

